A Bit of Analysis on Self-Timed Single-Bit On-Chip Links

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May 21, 2013

Single-Bit Interconnect

- Transmit data across die(s)
- How best to do that?
- Scope
  - Single-bit links
  - Asynchronous context
  - Delay-Insensitive Encodings
  - Handshaked links

Interconnect Design Challenges

- Pressure on Wiring Resources
  - Planar wiring (mostly) plentiful
  - Interconnect heavy-designs (FPGAs, etc)
  - Thru-Silicon Vias (TSVs) comparatively scarce
  - Delay-insensitive encodings expensive
- Electrical Characteristics
  - RC characteristics not scaling well
  - Lumped capacitance model invalid
  - Long wires — charge relaxation problem

Efficient Wire Usage

- Synchronous Most Wire-Count Efficient
  - Bundled data, etc. are close
  - Delay insensitive encodings worse
- Asynchronous Protocols Contextually Appropriate
  - 2-phase computation difficult
  - 4-phase dual-rail long distance signaling expensive

Choosing a Protocol

- What does "optimal" mean?
  - Area
  - Energy
  - Throughput
  - Latency
  - Ease of design
  - Robustness
- Approaching Optimality
  - Sizing
  - Circuit family
  - Buffer insertions
  - Metallization choices

Pareto Front

- Three Metrics
  - Throughput
  - Energy
  - Area
- Best Tradeoff

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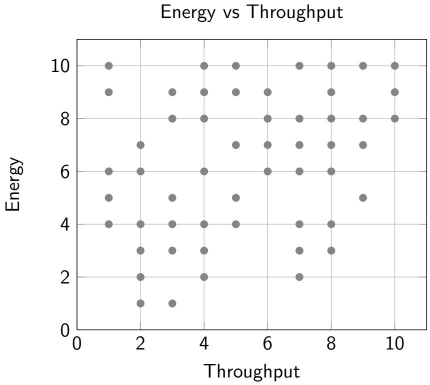

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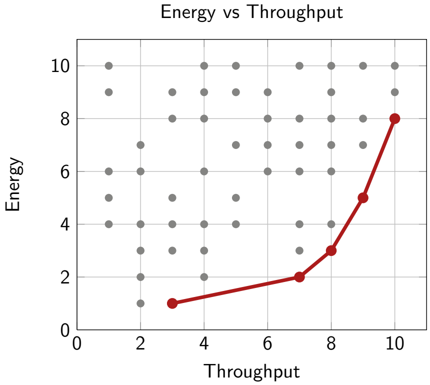

Single-Bit Links

Link	Handshake	Timing	Voltage	Wires
WCHB	4-Phase	QDI	Full-Swing	3
RQDI	2-Phase NRTN	RQDI	Full-Swing	3
STFB	2-Phase RTN	Single-Track	Full-Swing	2
ATLS	4-Phase	QDI	Ternary	2
STATS	2-Phase RTN	Single-Track	Ternary	1

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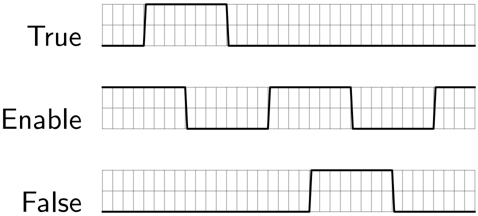

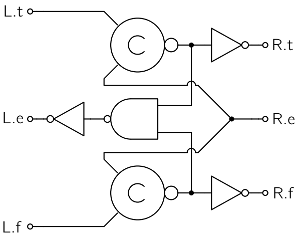

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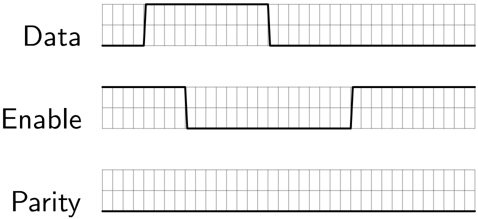

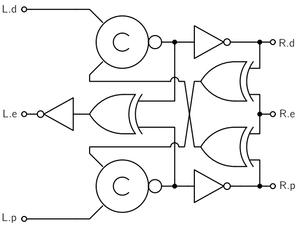

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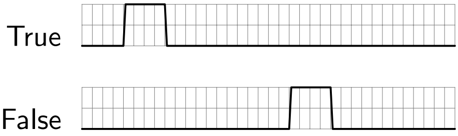

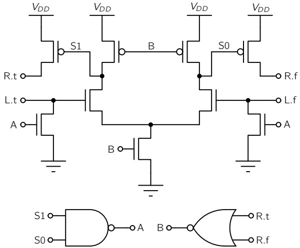

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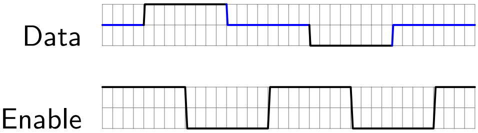

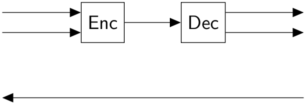

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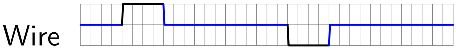
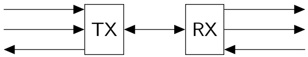
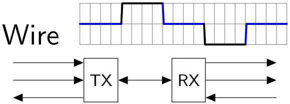




Single Track Asynchronous Ternary Signaling (STATS)



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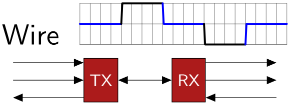

- $\frac{1}{2} V_{DD}$ Supply

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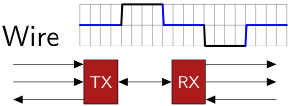

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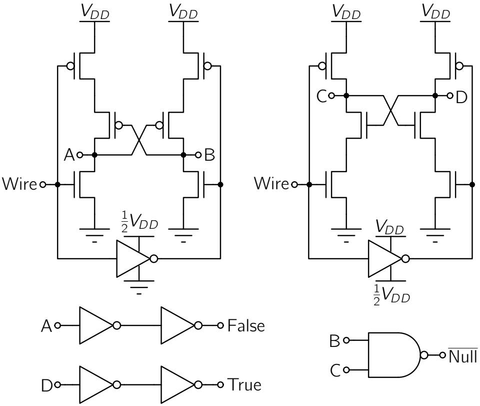

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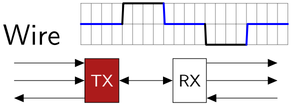
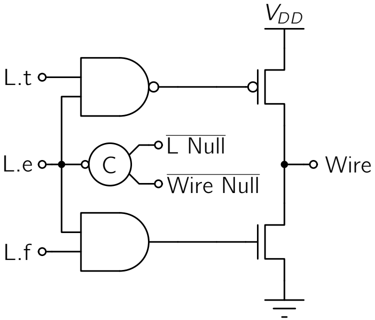


- $\frac{1}{2}V_{DD}$ Supply
- Ternary Decode
- Sending Tokens



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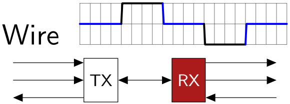
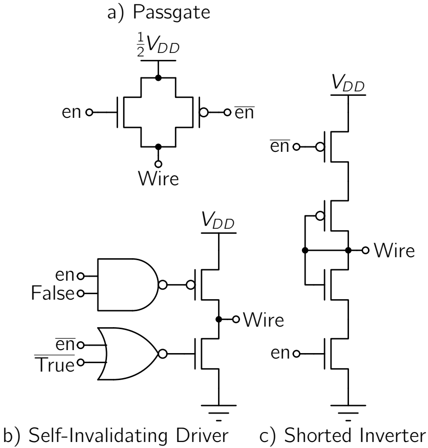


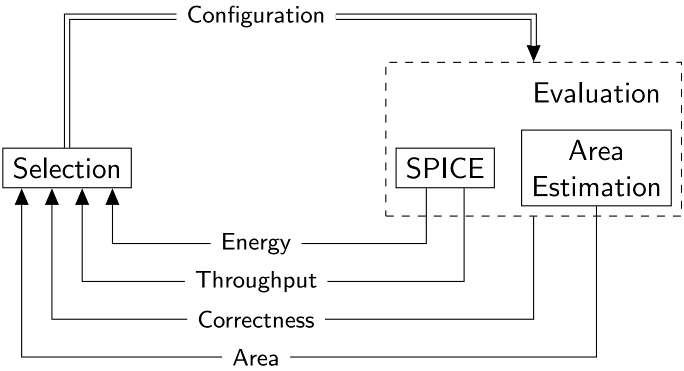
- $\frac{1}{2}V_{DD}$ Supply
- Ternary Decode
- Sending Tokens
- Return to Null



Heuristic Optimization

- Global Optimum?
  - Sizing problem is convex
  - Other non-sizing factors to consider
- Heuristic Optimization Techniques
  - General-purpose
  - Non-convex problems
  - Handles local optima
  - Flexible
  - Easy implementation

Genetic Algorithms

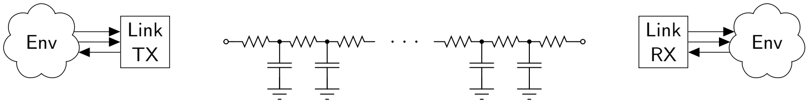


Evaluation

- Planar Wiring and TSV Cases
- 4-phase Dual-Rail Environment
- Configurations
  - Sizing
  - Circuit Topology
  - V_{DD} Scaling (Non-Ternary)
- Metrics
  - Throughput
  - Energy
  - Area

Planar Evaluation

- Distributed RC Wiring Model
- Dual-Rail Source/Sink
- Insert Buffers



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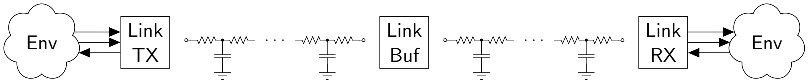
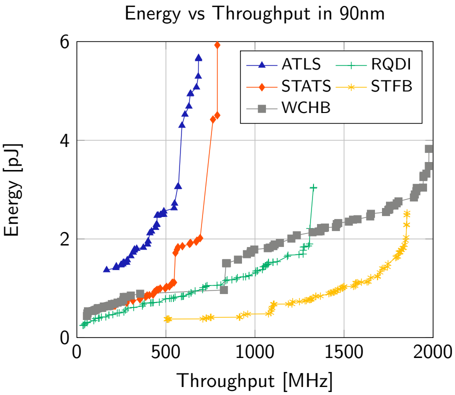
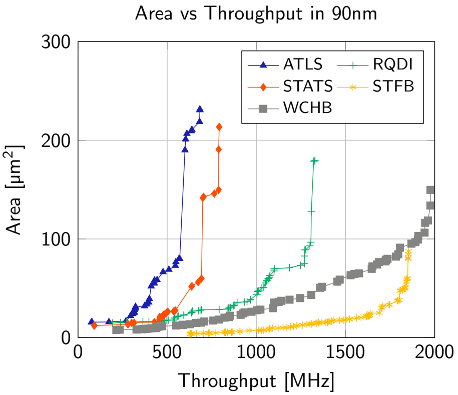
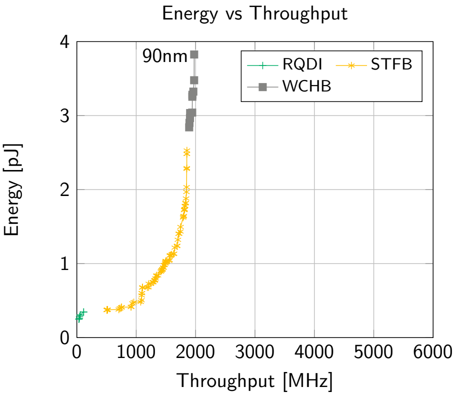


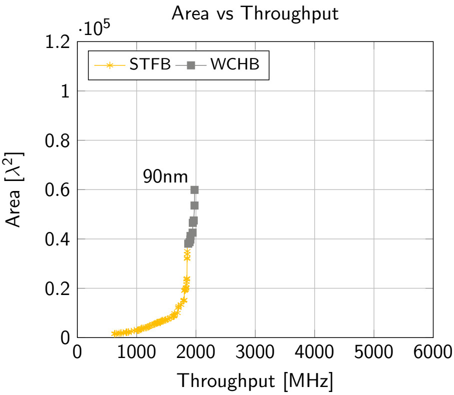
Planar Results in 90nm





Cross-Technology Planar Results





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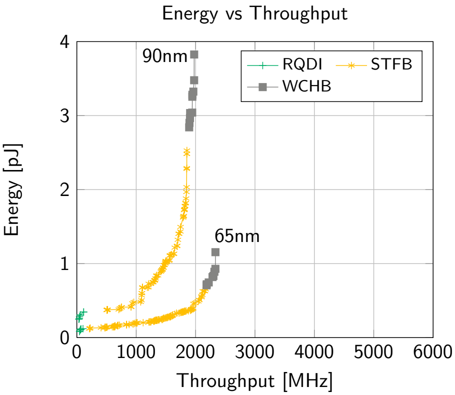

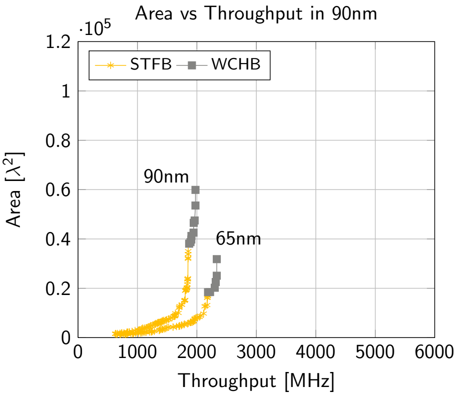

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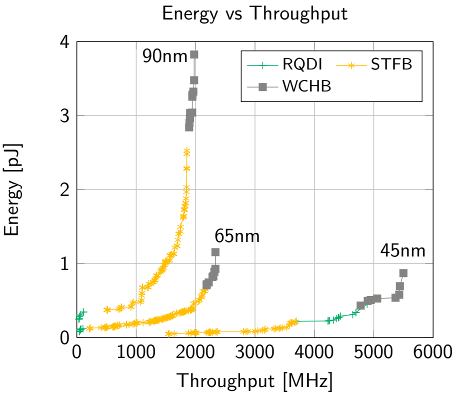
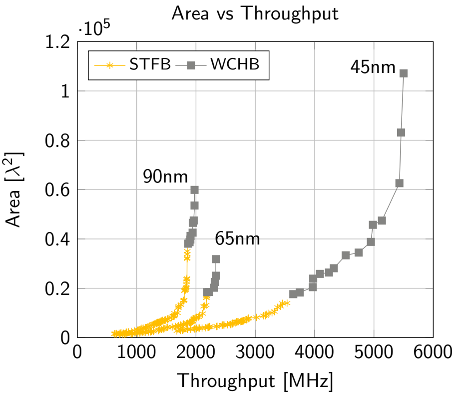


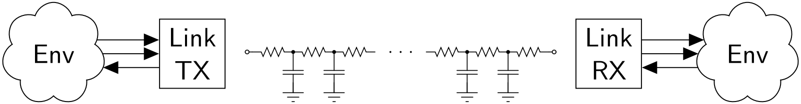


Planar Takeaway Points

- Single-Track Timing Assumption
  - STFB offers benefits in Energy, Area
  - WCHB, RQDI more conservative
- Ternary buffers are expensive
  - Perform poorly in high-resistance environments
  - Ternary conversion cost high

TSV Evaluation

- Pair of Buffers
- No Intermediary Buffers
- TSVs
  - Doesn't scale with technology
  - Less dense than planar
  - Wire-efficiency important
  - Scale throughput by TSV usage



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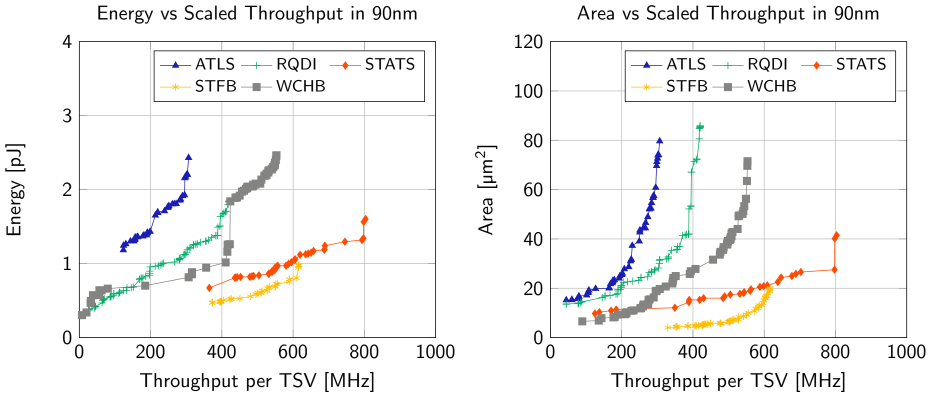

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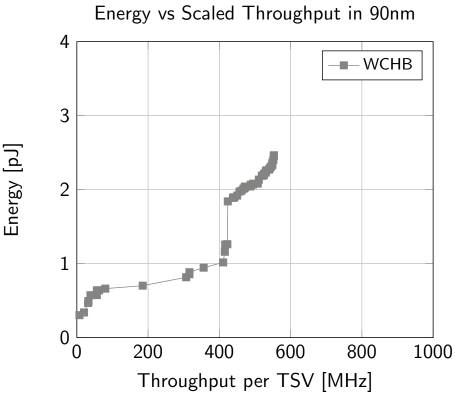
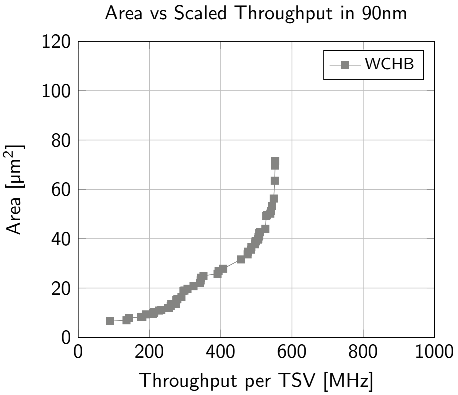
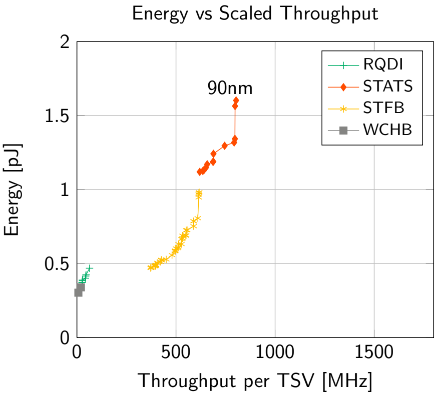
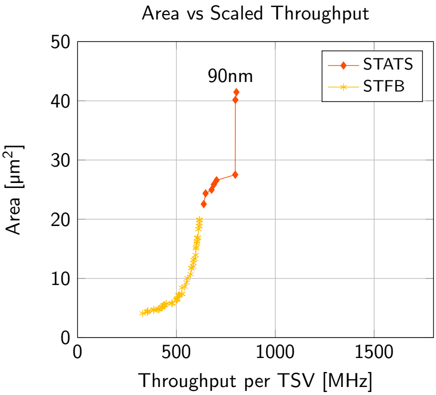




Cross-Technology TSV Results





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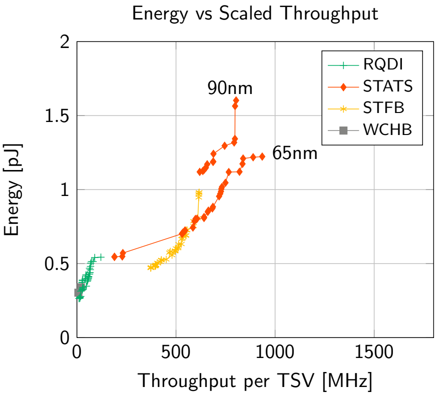

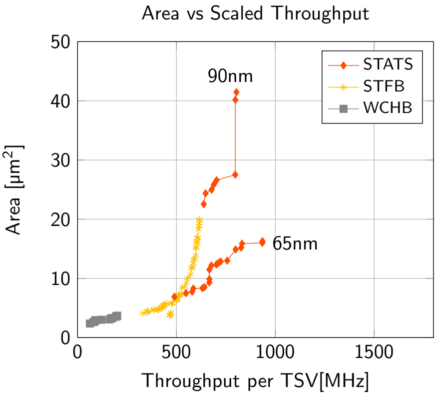

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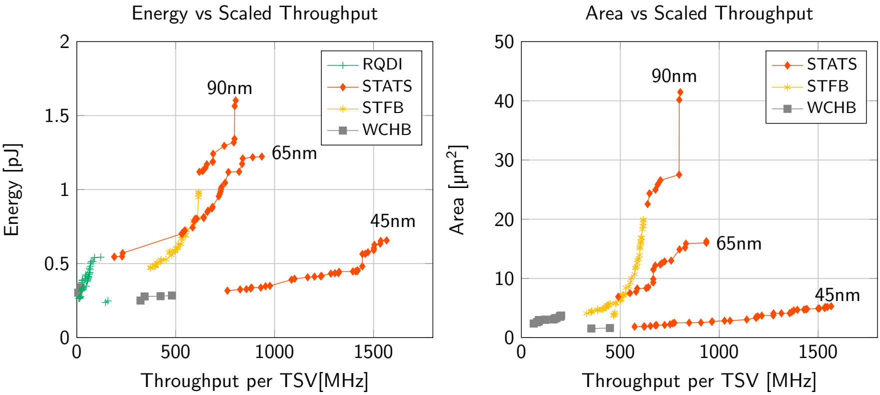

TSV Takeaway Points

- TSVs are highly capacitive
  - STATS good fit
  - STFB unhappy
- STATS efficiently uses TSVs
- Interesting optimization opportunities

Conclusion

- Single-Track Timing
  - Aggressive designs offer clear benefits
  - Difficult to design
  - Not as robust
- Full-QDI
  - WCHB is most robust
  - Small penalty for robustness
- Heuristic Optimization
  - Quick design-space exploration
  - Augment/confirm designer intuition
  - Flexible, easy to implement
  - Pareto front tradeoff

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Link Failure Rates

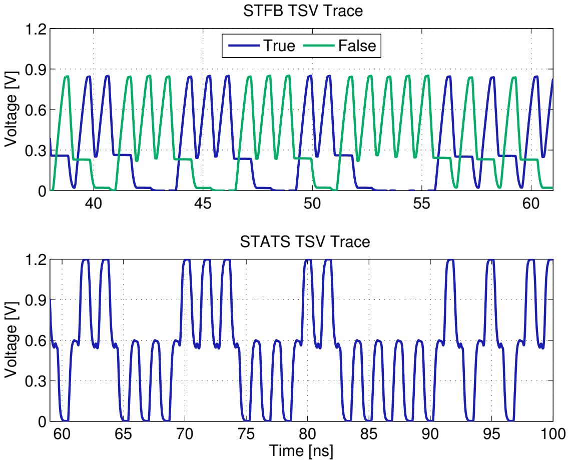
Link	% Planar Failure			% TSV Failure		
	90 nm	65 nm	45 nm	90 nm	65 nm	45 nm
ATLS	23.94	16.34	19.23	17.72	20.83	15.54
RQDI	25.60	23.93	17.80	19.72	21.52	24.68
STATS	42.40	36.26	45.45	33.26	33.96	33.31
STFB	28.18	21.99	33.63	29.19	99.33	100.00
WCHB	10.67	8.49	12.43	12.79	12.80	25.32

Note: $2856 \leq n \leq 11158$

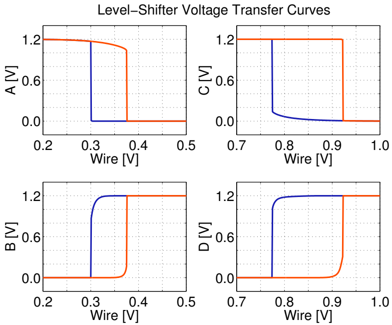
Average Sparse Wiring Energy Percentage Improvements

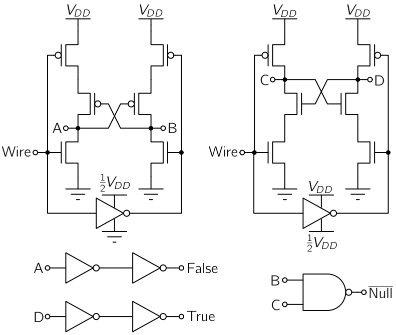
Link	90 nm	65 nm	45 nm
ATLS	47.36	16.93	-24.67
RQDI	33.71	7.22	13.98
STATS	27.42	-92.28	-112.87
STFB	39.04	18.11	12.26
WCHB	49.66	28.43	20.99

Single-Track Trace



Noise Margin





WCHB Level Shifters